FIG. 1

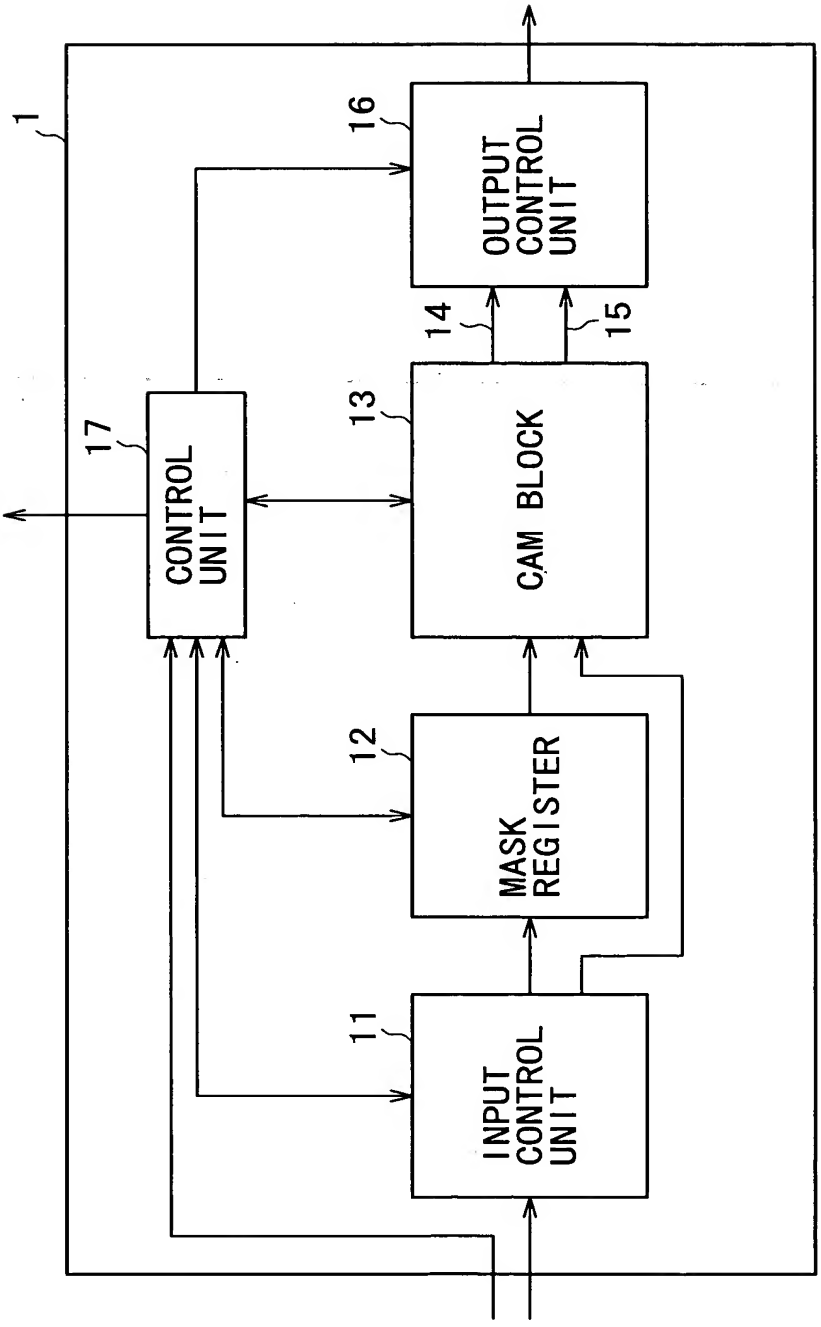
1
16
OUTPUT CONTROL UNIT
14
15
13
CAM BLOCK
17
CONTROL UNIT
12
MASK REGISTER
11
INPUT CONTROL UNIT

FIG. 2

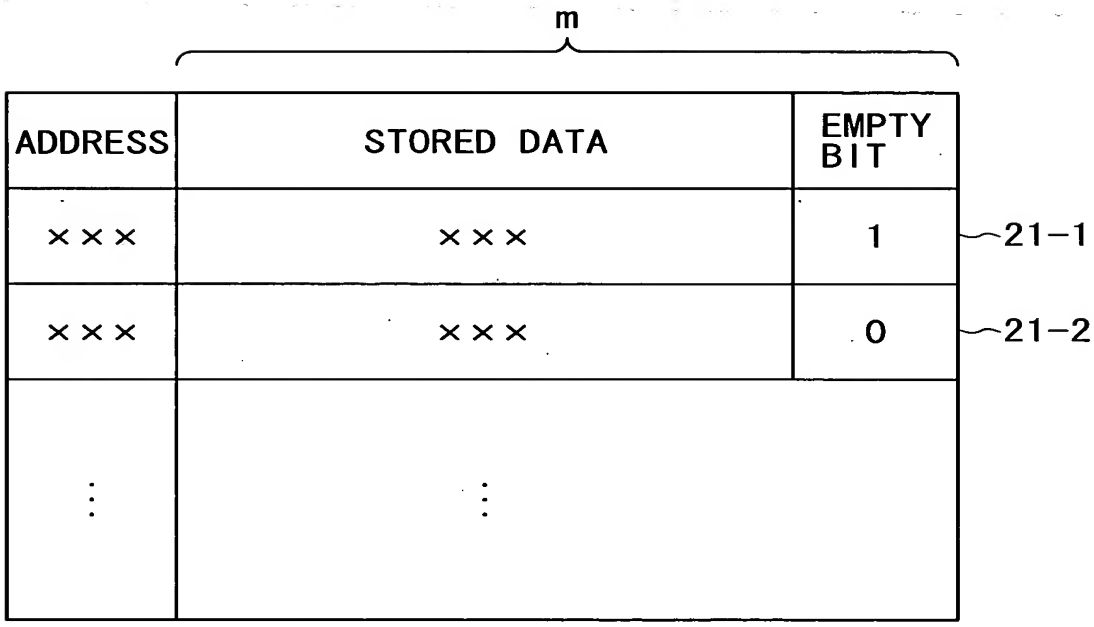

FIG. 3

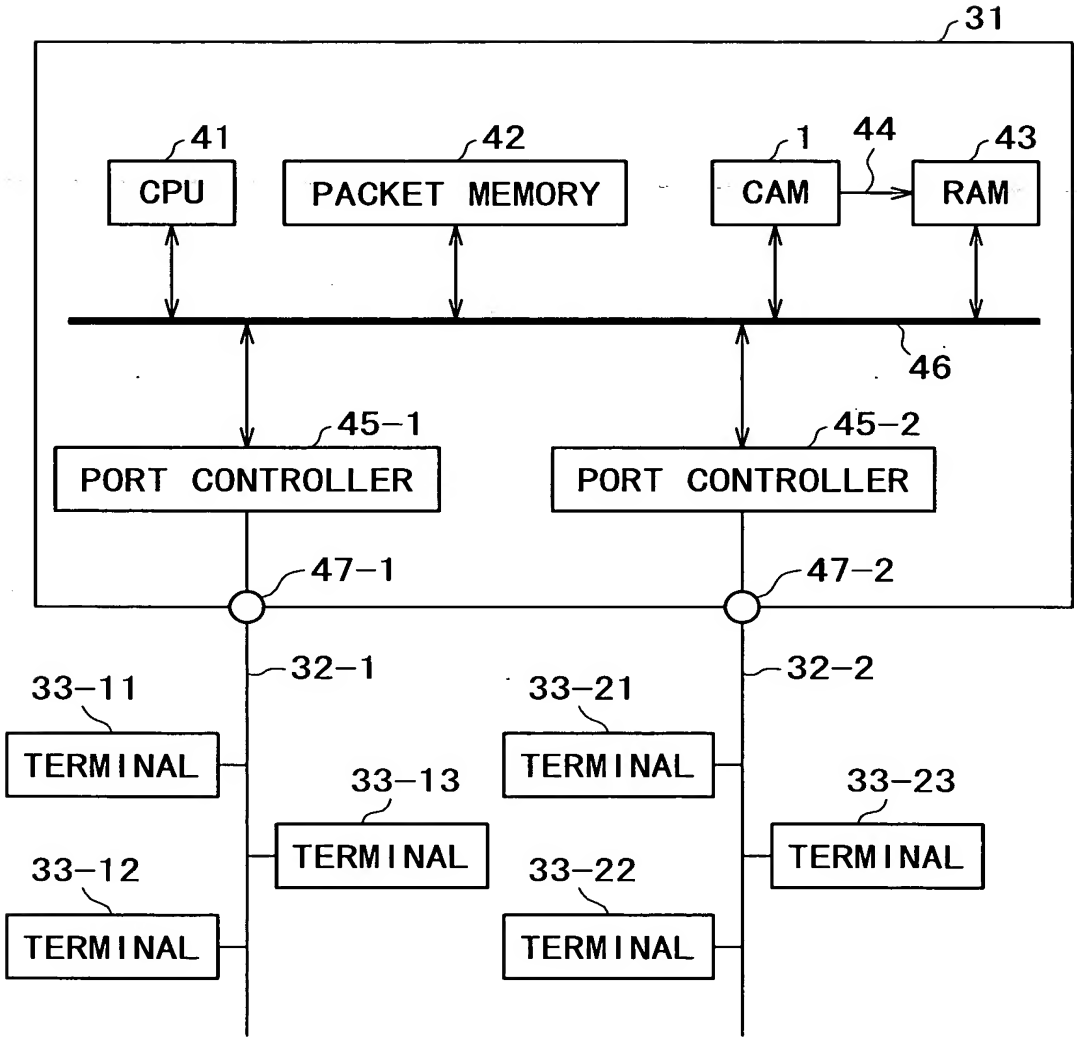
31
41
CPU
42
PACKET MEMORY
1
44
CAM
43
RAM
46
45-1
PORT CONTROLLER
45-2
PORT CONTROLLER
47-1
47-2
32-1
32-2
33-11
TERMINAL
33-21
TERMINAL
33-13
TERMINAL
33-23
TERMINAL
33-12
TERMINAL
33-22
TERMINAL

FIG. 4

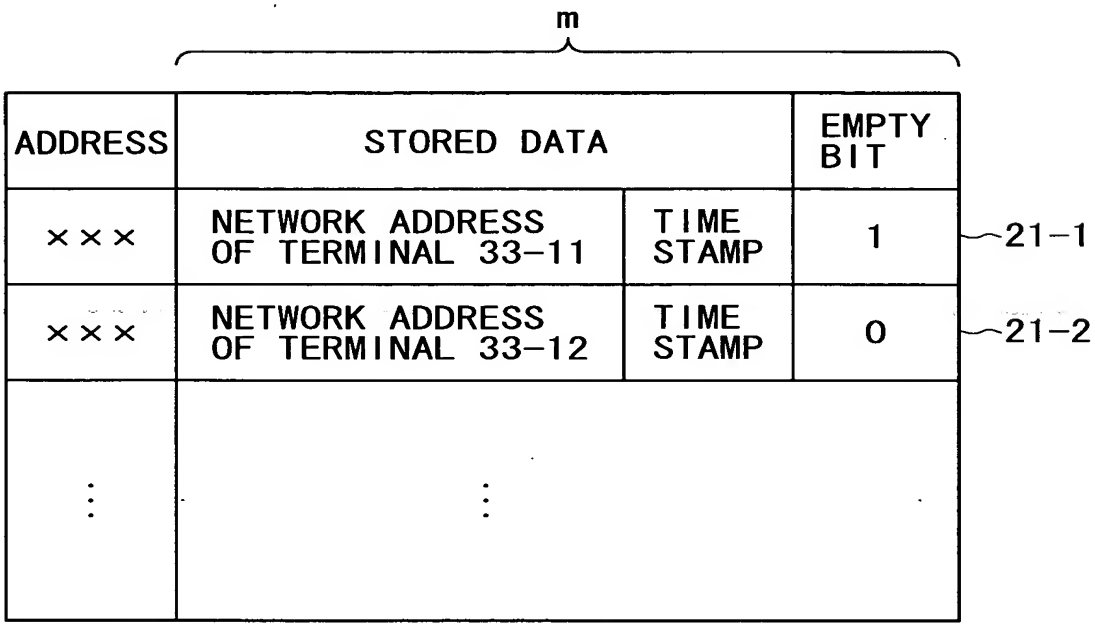
m
ADDRESS
STORED DATA
EMPTY BIT
×××
NETWORK ADDRESS OF TERMINAL 33-11
TIME STAMP
1
21-1
×××
NETWORK ADDRESS OF TERMINAL 33-12
TIME STAMP
0
21-2

FIG. 5

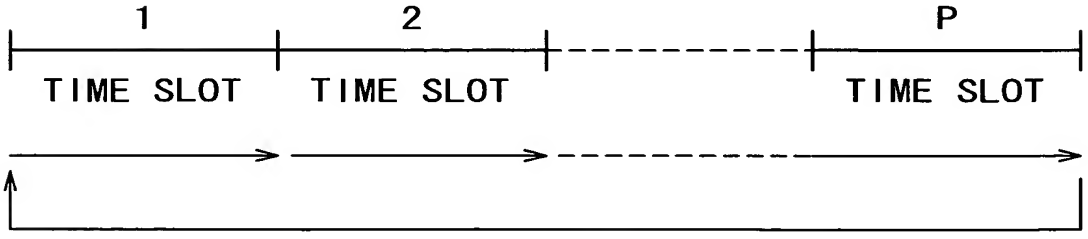
1
2
P
TIME SLOT
TIME SLOT
TIME SLOT

FIG. 6

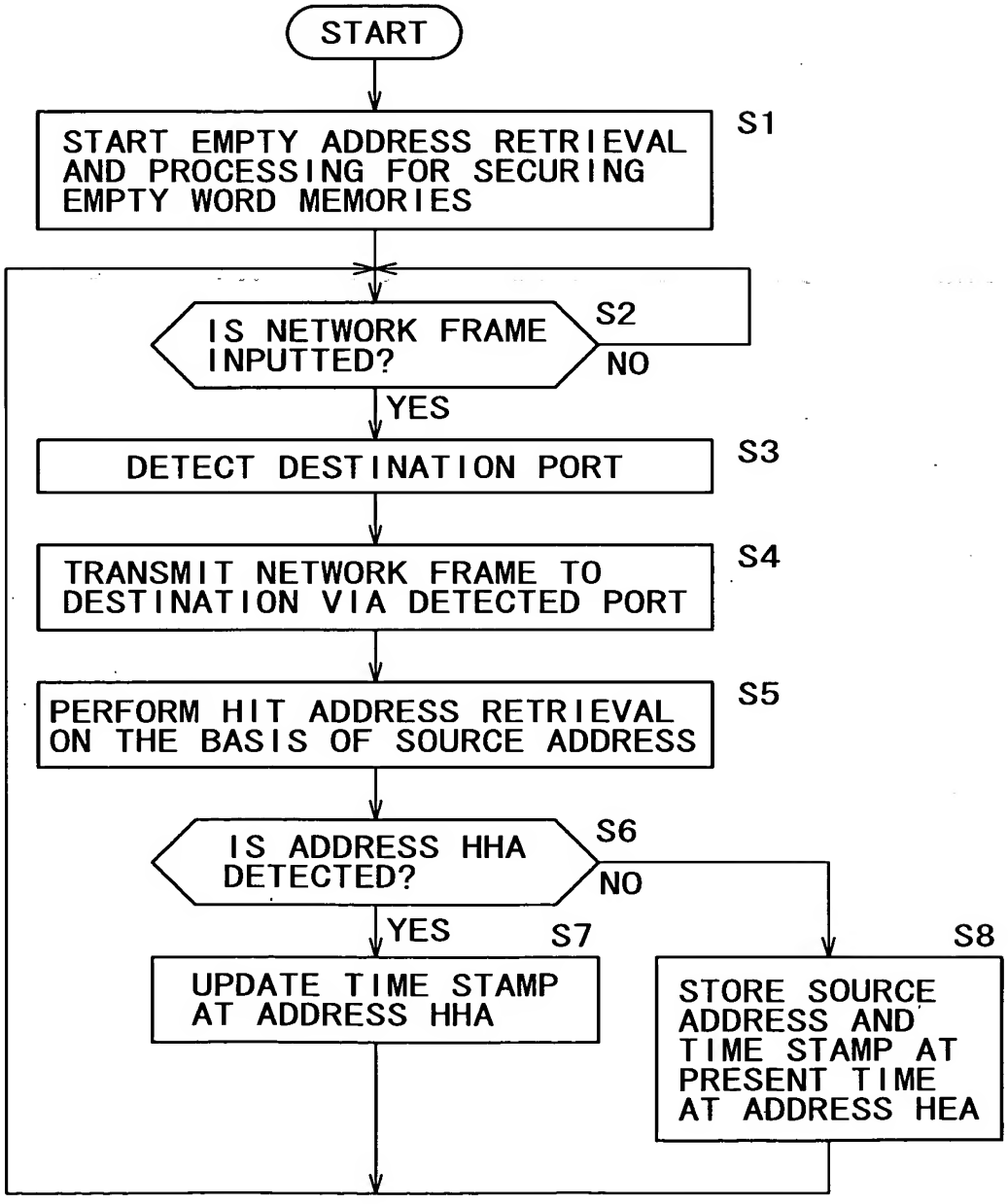
START
START EMPTY ADDRESS RETRIEVAL AND PROCESSING FOR SECURING EMPTY WORD MEMORIES
S1
IS NETWORK FRAME INPUTTED?
S2
NO
YES
DETECT DESTINATION PORT
S3
TRANSMIT NETWORK FRAME TO DESTINATION VIA DETECTED PORT
S4
PERFORM HIT ADDRESS RETRIEVAL ON THE BASIS OF SOURCE ADDRESS
S5
IS ADDRESS HHA DETECTED?
S6
NO
YES
S7
UPDATE TIME STAMP AT ADDRESS HHA
S8
STORE SOURCE ADDRESS AND TIME STAMP AT PRESENT TIME AT ADDRESS HEA

FIG. 7

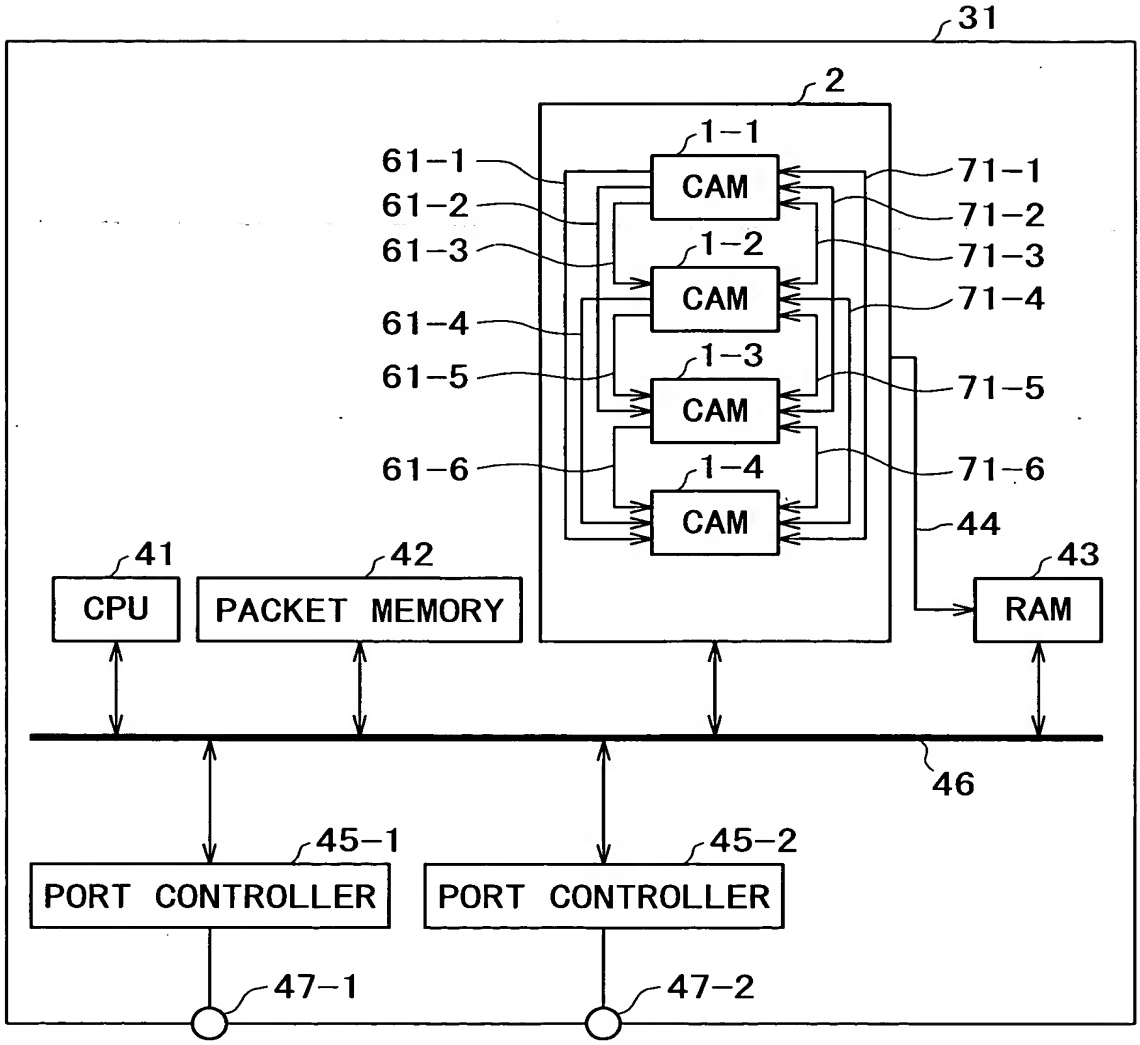
31
2
1-1
CAM
1-2
CAM
1-3
CAM
1-4
CAM
61-1
61-2
61-3
61-4
61-5
61-6
71-1
71-2
71-3
71-4
71-5
71-6
44
41
CPU
42
PACKET MEMORY
43
RAM
46
45-1
PORT CONTROLLER
45-2
PORT CONTROLLER
47-1
47-2

FIG. 8

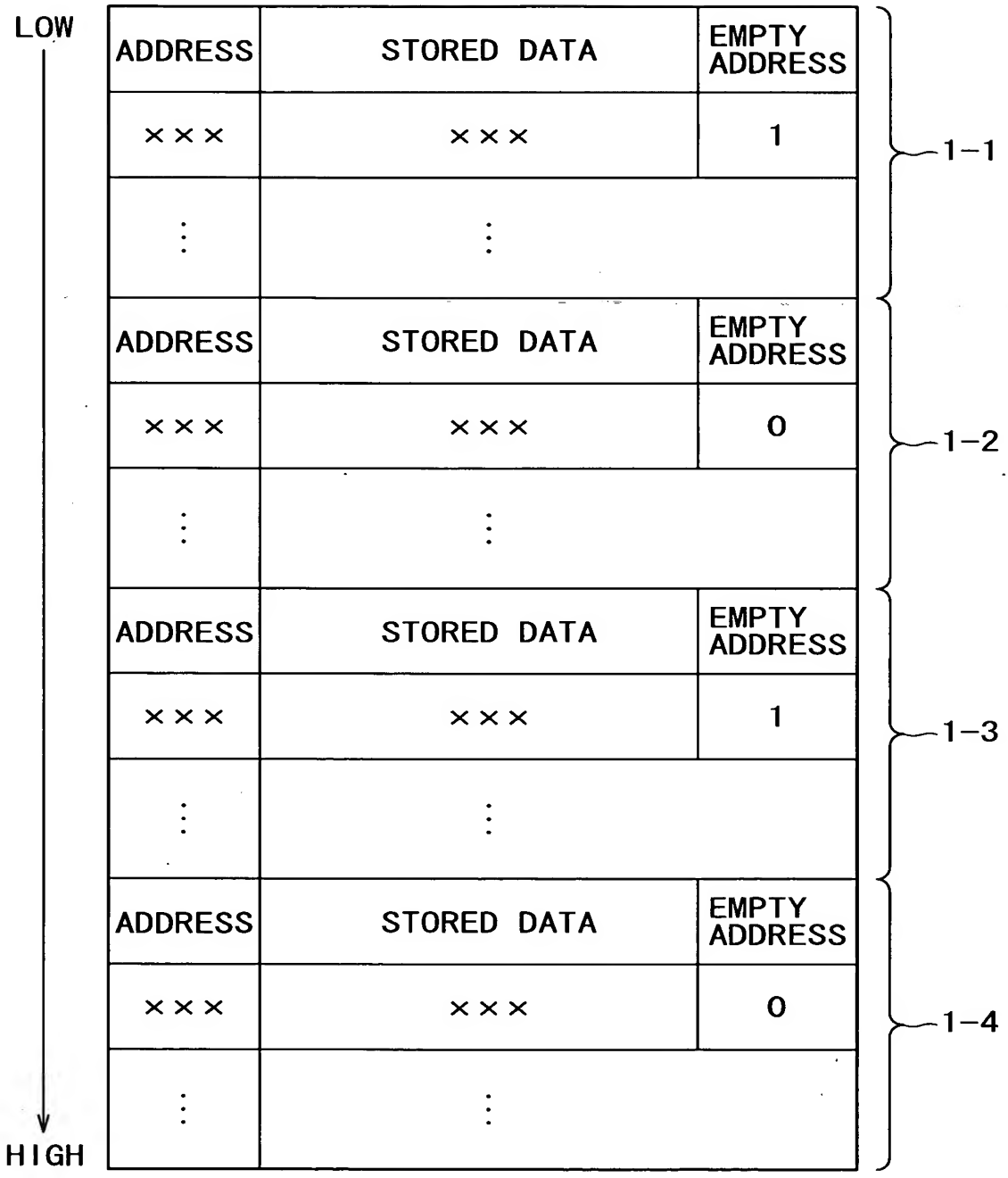

FIG. 9

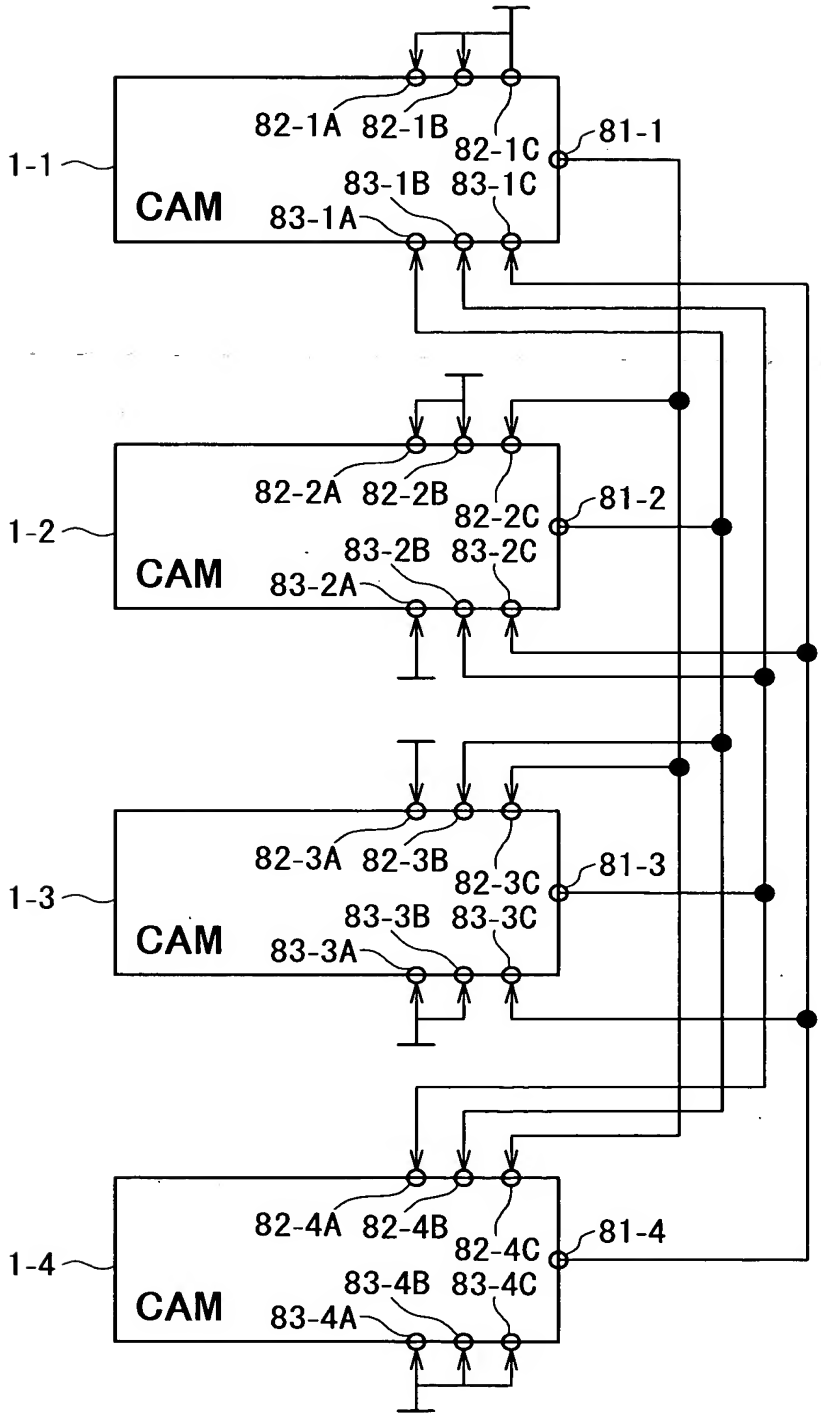
1-1
CAM
82-1A
82-1B
82-1C
81-1
83-1A
83-1B
83-1C
1-2
CAM
82-2A
82-2B
82-2C
81-2
83-2A
83-2B
83-2C
1-3
CAM
82-3A
82-3B
82-3C
81-3
83-3A
83-3B
83-3C
1-4
CAM
82-4A
82-4B
82-4C
81-4
83-4A
83-4B
83-4C

FIG. 10

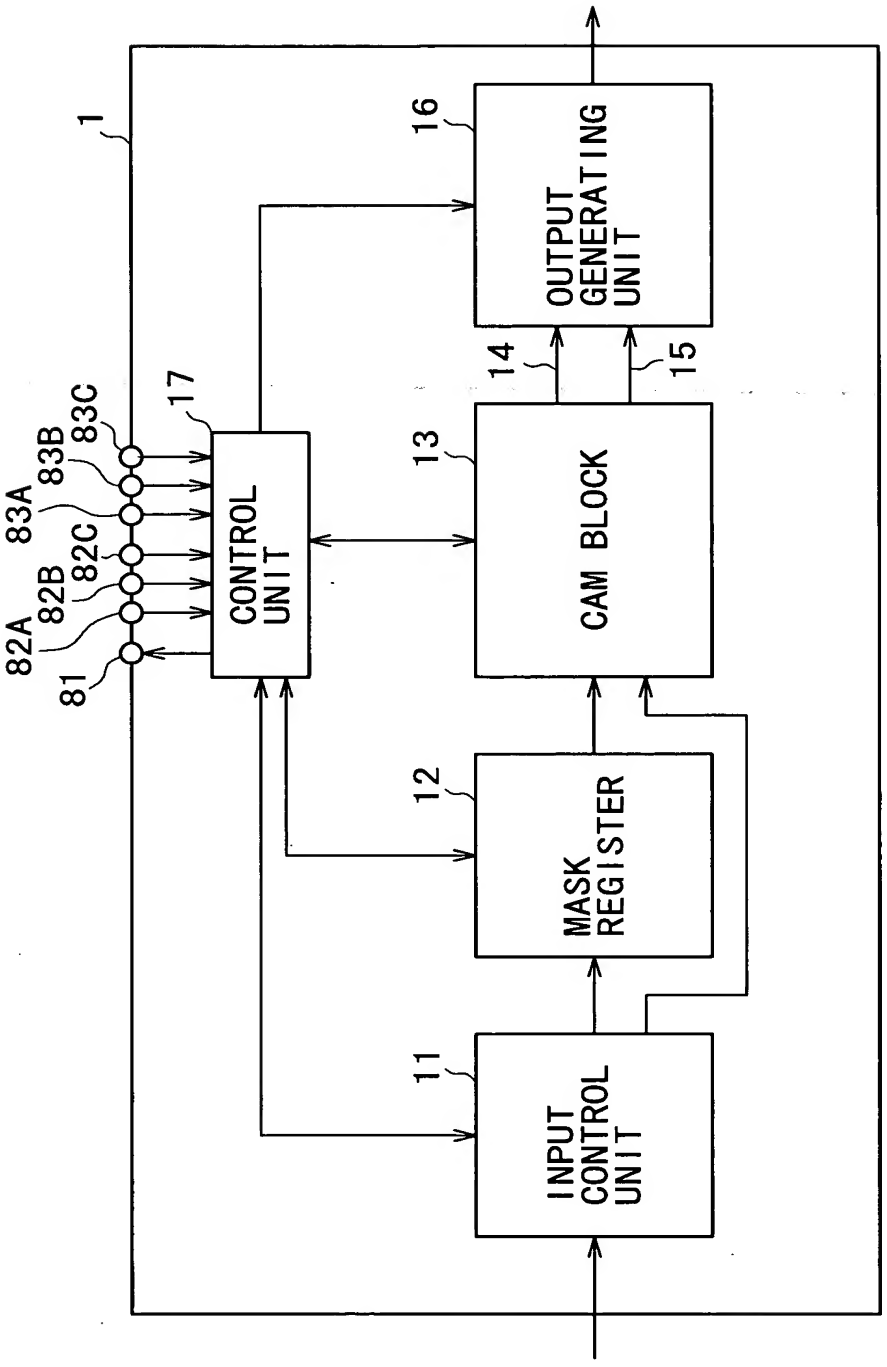
1
16
OUTPUT GENERATING UNIT
14
15
17
83C
83B
83A
82C
82B
82A
81
CONTROL UNIT
13
CAM BLOCK
12
MASK REGISTER
11
INPUT CONTROL UNIT

FIG. 11

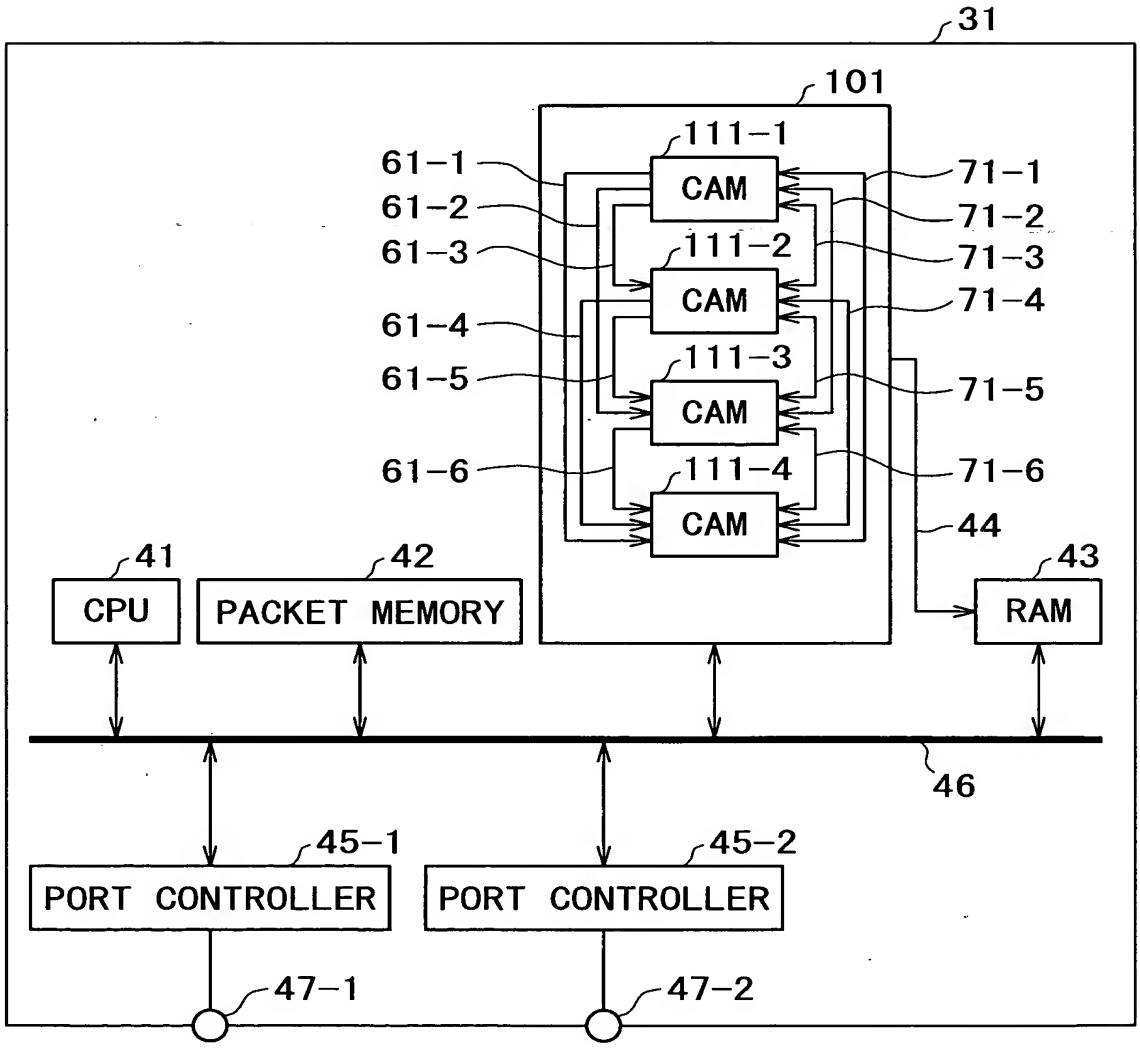
31
101
111-1
CAM
111-2
CAM
111-3
CAM
111-4
CAM
61-1
61-2
61-3
61-4
61-5
61-6
71-1
71-2
71-3
71-4
71-5
71-6
44
41
CPU
42
PACKET MEMORY
43
RAM
46
45-1
PORT CONTROLLER
45-2
PORT CONTROLLER
47-1
47-2

FIG. 12

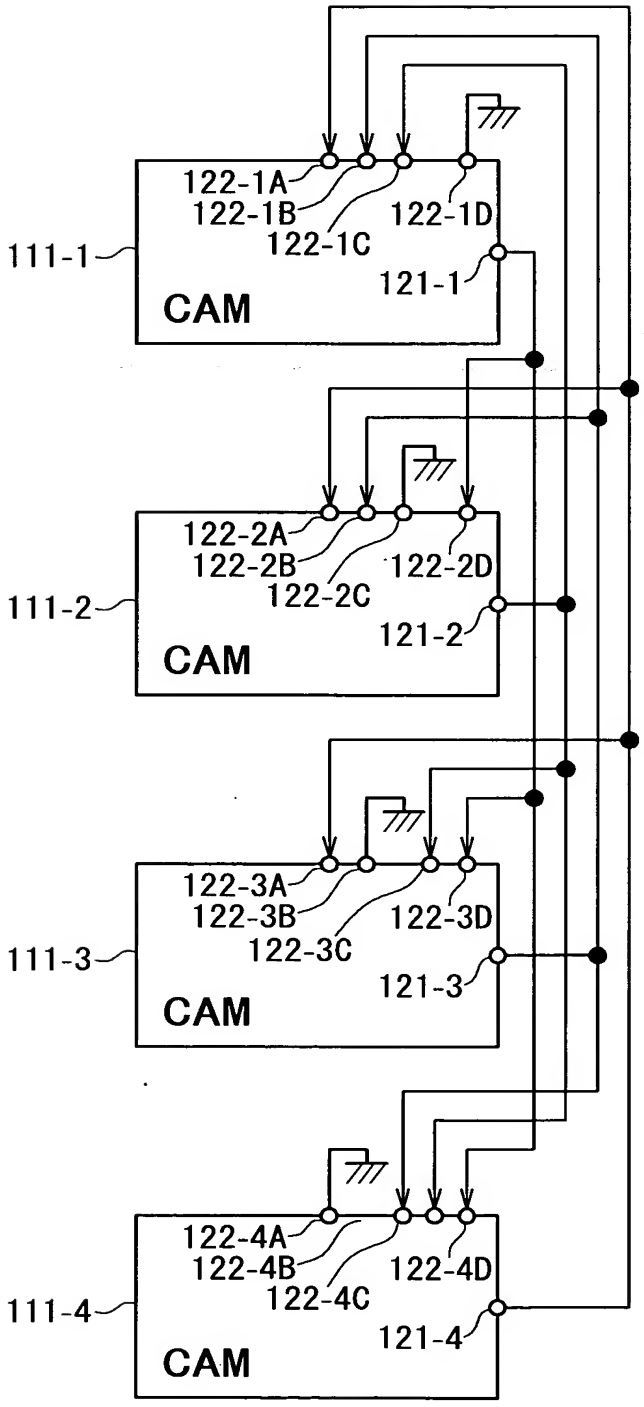
111-1
CAM
122-1A
122-1B
122-1C
122-1D
121-1
111-2
CAM
122-2A
122-2B
122-2C
122-2D
121-2
111-3
CAM
122-3A
122-3B
122-3C
122-3D
121-3
111-4
CAM
122-4A
122-4B
122-4C
122-4D
121-4

FIG. 13

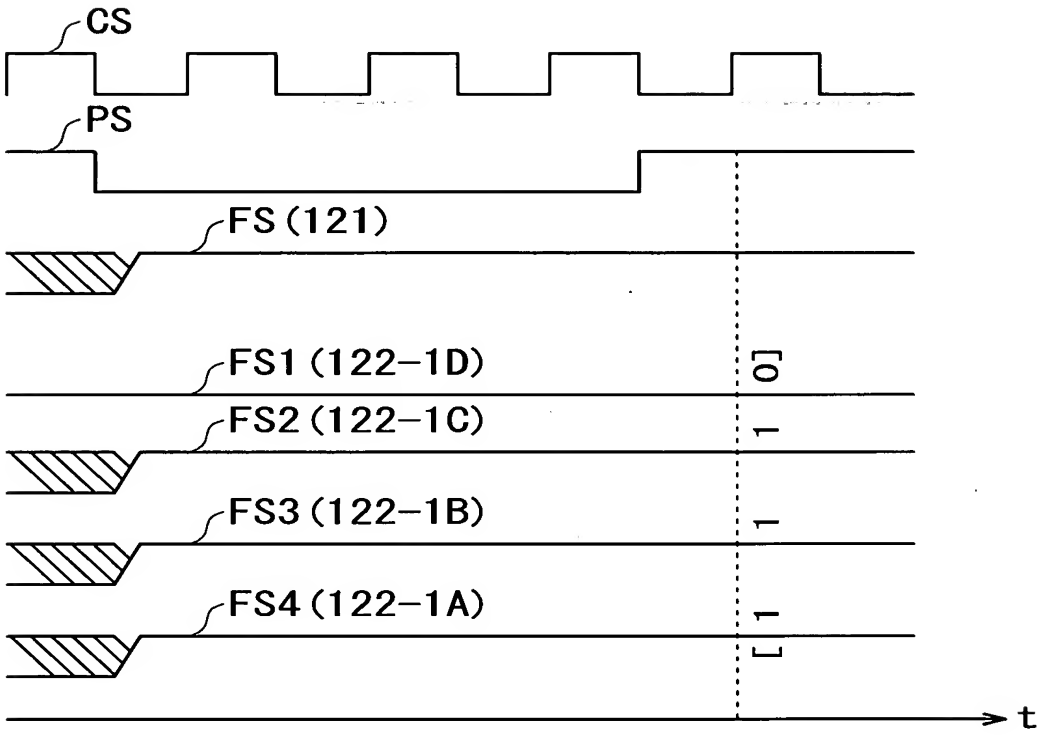

FIG. 14

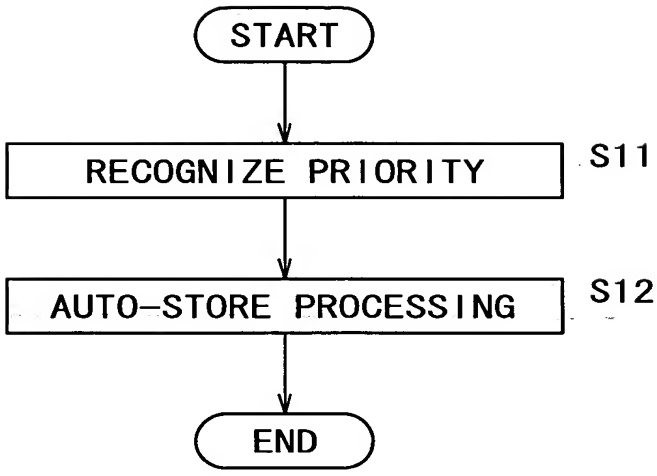

FIG. 15

INPUT SIGNAL [ABCD]	PROCESSING
[1110]	INTERNAL HIT
[1101]	INPUT SIGNAL[D]!=0&&, INTERNAL HIT
[1011]	INPUT SIGNAL[C]!=0&&, INPUT SIGNAL[D]!=0&& INTERNAL HIT
[0111]	INPUT SIGNAL[B]!=0&&, INPUT SIGNAL[C]!=0&& INPUT SIGNAL[D]!=0&&, INTERNAL HIT

FIG. 16

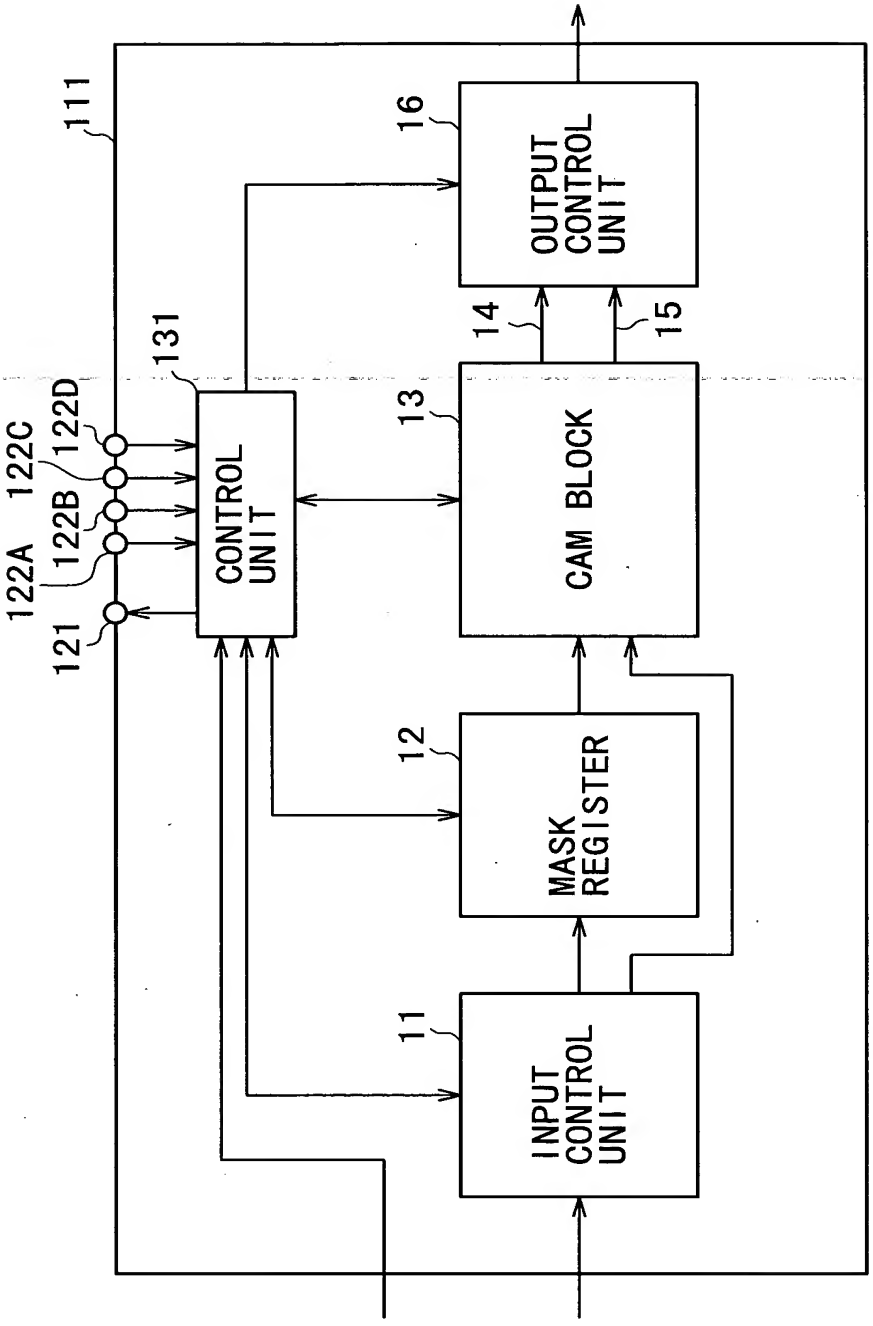
111
16
OUTPUT CONTROL UNIT
131
14
15
122D
122C
122B
122A
121
CONTROL UNIT
13
CAM BLOCK
12
MASK REGISTER
11
INPUT CONTROL UNIT

FIG. 17

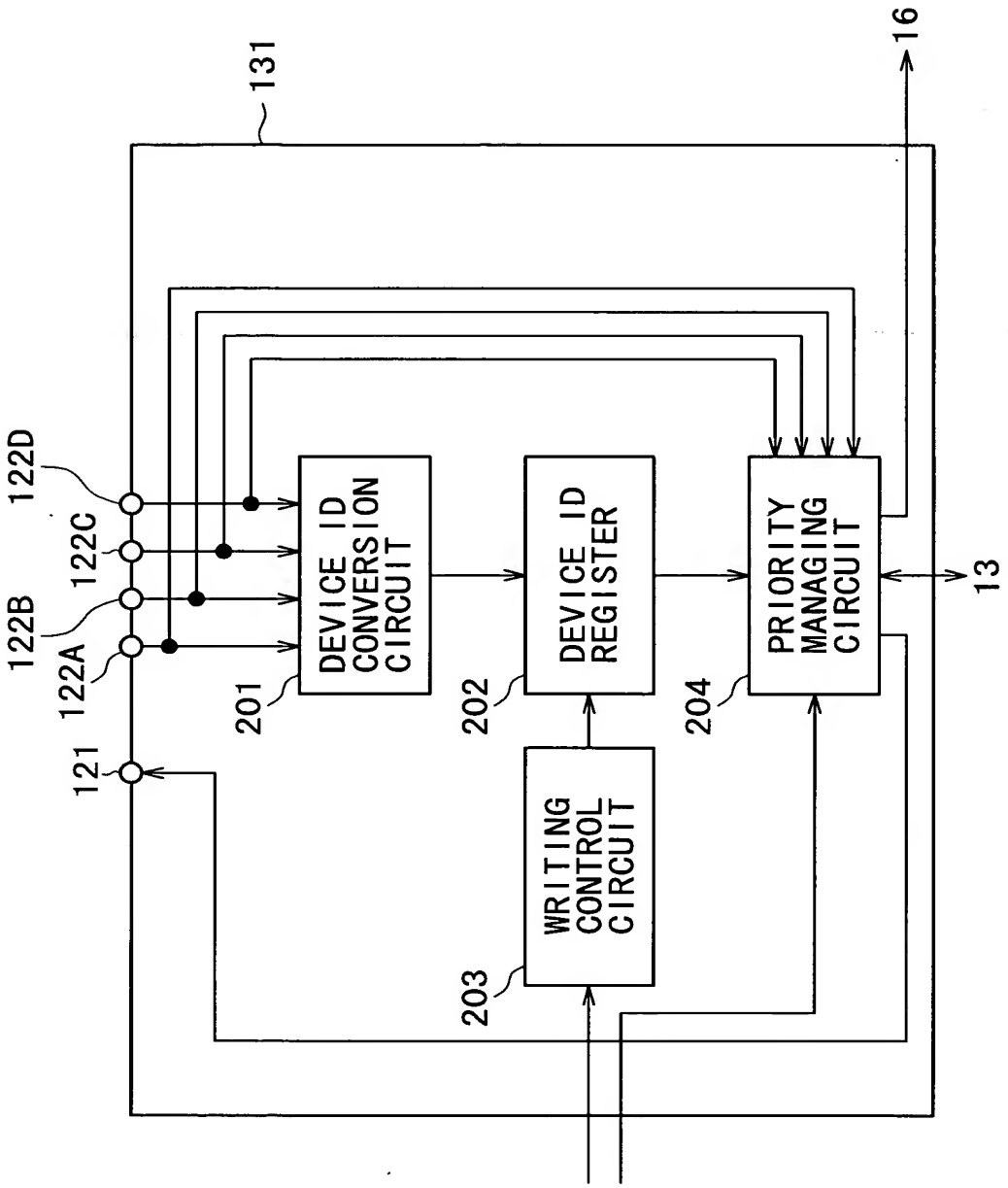
131
16
122D
122C
122B
122A
121
DEVICE ID CONVERSION CIRCUIT
201
DEVICE ID REGISTER
202
PRIORITY MANAGING CIRCUIT
204
13
WRITING CONTROL CIRCUIT
203

FIG. 18

INPUT SIGNAL [ABCD]	DEVICE ID
[1110]	0
[1101]	1
[1011]	2
[0111]	3